UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,877	07/15/2003	Eric N. Paton	039153-0642 (H0970)	7818

26371 7590 03/29/2004

FOLEY & LARDNER
777 EAST WISCONSIN AVENUE
SUITE 3800
MILWAUKEE, WI 53202-5308

EXAMINER	
VOCKRODT, JEFF B	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,877	PATON ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the application papers filed on July 15, 2003. Claims 1-20 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,998,807 ("Lustig").

Claim 17. Claims are given their broadest reasonable interpretation in the USPTO. The steps of claim 17 need not be performed in their written order to be met by the prior art. Specifically, the step of "providing spacers for the first set of gate structures" can be performed at any stage of the process. Additionally, the "comprising" transitional phrase opens the claim to processes that also provide spacers for the second set of gate structures as well as the first set. That is to say, claim 17 does not require selectively providing spacers for a second group as does claim 11.

Lustig teaches forming gate structures (10/11/12) on a strained silicon layer (5); providing spacers (140) for the first set of gate structures (Fig. 3); covering the first set of gate

structures (with mask 15, Fig. 3); forming deep S/D regions (16) for the second gate (Fig. 3); removing the mask 15 (Figs. 3-4); covering the second set of gate structures (with 2d mask 17, Fig. 4); forming deep S/D regions (18) for the first gate structures (Fig. 4).

Claim 18. A tempering step is performed for 60 seconds at 800°C (col. 5, ll. 10-11).

Claim 19. The strained silicon layer (5) is formed above a Si-Ge layer (4).

Claim 20. The deep S/D regions are provided by implantation (col. 5, ll. 1-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,141,890 ("Haken") in view of US 6,649,492 ("Chu").

Claim 11. The preamble of claim 11 "ultra-large scale" is given little patentable weight as it relates to a statement of purpose or intended use.

Haken teaches providing deep source drain regions ("p+ implant," Fig. 2) selectively for a first set of transistors; selectively forming oxide spacers ("sidewall oxide," Fig. 3) for a second, different set of transistors; wherein the first and the second group are provided on a top surface of a strained semiconductor layer; and selectively providing S/D regions for the second group ("N + S/D," Fig. 3).

As noted by the underlining above, claim 11 differs from Haken in the manner of the substrate used. Modifying Haken such that the silicon layer is strained would produce (i.e., meet each limitation of) the claimed invention.

Chu teaches that applying conventional CMOS process flows to strained silicon base layers was known to enhance the transport for both holes and electrons (col. 4, ll. 49-57). Chu further notes that the advantages of the strained silicon layer will accrue to many technologies (col. 10, ll. 4-15). Thus, there is no reason to believe that the transport properties of the device of Haken would not benefit from being formed on a strained silicon layer as well.

A person of ordinary skill in the art would have reasonably expected that incorporating a strained silicon base layer into the device of Haken would lead to an improvement in transport for both holes and electrons. Thus, the claimed invention would have been prima facie obvious to a person having ordinary skill in the art at the time of the invention.

Claims 14-15. The strained silicon layer of Chu contains silicon, which is positioned above a Si-Ge layer.

Claim 16. Haken teaches a 3000 angstrom thick LPCVD oxide for forming the spacers on a 5000 angstrom poly layer (the spacer height corresponding to the gate height due to the self aligned process). The width of the spacers is a results effective variable as it determines the channel length and must shrink as channel length decreases. Official notice is taken that in the channel length of CMOS devices generally shrinks with each new generation of devices and that this reduction in size is desirable. Accordingly, a person of ordinary skill in the art would have been motivated to use thinner spacers in order to keep the channel length in line with the general trend in device fabrication.

Claims 1, 7, 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,654,212 ("Jang") in view of US 6,649,492 ("Chu").

Claim 1. Claims are given their broadest reasonable interpretation in the USPTO. The steps of claim 1 need not be performed in their written order to be met by the prior art. Specifically, the step of "providing a second spacer to the first gate structure" can be performed

at any stage of the process. Additionally, the "comprising" transitional phrase opens the claim to processes that also provide spacers for the second set of gate structures as well as the first set. That is to say, claim 1 does not require selectively providing spacers for a second group as does claim 11.

Jang teaches providing first and second gates each with a sidewall spacer (260, Fig. 2D); providing a first mask (262, Fig. 2E) over a first area; forming deep S/D regions (275) in the second area; removing the first masking layer (262, Figs. 2E-2F); providing a second spacer (265) to the first gate structure (Fig. 2F); masking the second region with a mask (277, Fig. 2G); forming second deep S/D regions (280) in the first area (note: claim actually says second here, but it looks like a mistake).

Claim 1 differs from Jang by requiring a strained silicon substrate, whereas Jang teaches a conventional silicon substrate.

Chu teaches that applying conventional CMOS process flows to strained silicon base layers was known to enhance the transport for both holes and electrons (col. 4, ll. 49-57). Chu further notes that the advantages of the strained silicon layer will accrue to many technologies (col. 10, ll. 4-15). Thus, there is no reason to believe that the transport properties of the device of Jang would not benefit from being formed on a strained silicon layer as well.

A person of ordinary skill in the art would have reasonably expected that incorporating a strained silicon base layer into the device of Jang would lead to an improvement in transport for both holes and electrons as suggested by Chu. Thus, the claimed invention would have been prima facie obvious to a person having ordinary skill in the art at the time of the invention.

Claim 7. The gates are made of polysilicon in Jang.

Claim 8. Jang teaches covering portion of the substrate with an insulating layer (e.g., field oxide regions).

Claim 9. The width of the spacers is a results effective variable as it determines the channel length and must shrink as channel length decreases. Official notice is taken that in the channel length of CMOS devices generally shrinks with each new generation of devices and that this reduction in size is desirable. Accordingly, a person of ordinary skill in the art would have been motivated to use thinner spacers in order to keep the channel length in line with the general trend in device fabrication.

Claim 10. Claim 10 depends from 9 and specifies arsenic as the dopant for the second S/D. The second S/D is a N+ region. Official notice is taken that arsenic was a well known and desirable N+ dopant at the time of the invention. It would have been obvious to select arsenic for the N+ dopant in Jang since it was well known and desirable for use as a N+ dopant at the time of the invention.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang in view of Chu as applied to claims 1, 7, 8, 9, and 10 above, further in view of US 6,689,671 ("Yu").

Jang and Chu do not teach activating the source and drain regions at a temperature of less than 600°C.

Yu teaches that low temperature dopant activation is important for allowing relaxation of strained Si-Ge materials (¶ bridging cols. 6-7). Yu teaches an activation anneal performed at a temperature of 500-600°C for about 30 seconds (col. 6, ll. 18-25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use an anneal of between 500-600°C to activate the dopants in the process of Jang and Chu. Such modification would have been desirable because low temperature activation is desirable for strained semiconductor layers as taught by Yu.

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang, Chu, and Yu as applied to claims 2-3 above, further in view of US 5,624,871 ("Teo").

Jang and Chu do not teach how the photoresist mask is removed, or whether it is removed using dry etching.

Teo teaches that photoresist stripping (removal) is usually carried out by ashing, which is a dry etching process. (Teo, col. 6, ll. 33-37).

It would have been obvious to use dry etching to remove the photoresist in the process of Jang and Chu as conventional photoresist stripping (removal) using an ashing process is a type of dry etching as taught by Teo.

Claim 5. The spacers of Jang are formed from layer 255, which is either nitride or oxide.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jang in view of Chu as applied to claims 1, 7, 8, 9, and 10 above, further in view of US 5,384,285 ("Sitaram").

Jang and Chu collectively teach a CMOS process carried out on a strained silicon layer, but differ in that a silicide layer is not formed on the exposed source/drain regions and the exposed gate region.

Sitaram teaches a SALICIDE (self-aligned silicide) process in which regions 40, 42, and 44 are formed of silicide. Sitaram teaches that silicide lowers the contact resistance (col. 5, ll. 30-35; col. 5, ll. 40-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to form a silicide region over the source/drain and gate in the process of Jang and Chu. A person of ordinary skill in the art would have been motivated to do this by the expectation that such a modification would lower the contact resistance of the device as suggested by Sitaram.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haken and Chu as applied to claims 11 and 14-16 above, further in view of Sitaram.

Haken and Chu collectively teach a CMOS process carried out on a strained silicon layer, but differ in that a silicide layer is not formed on the exposed source/drain regions and the exposed gate region.

Sitaram teaches a SALICIDE (self-aligned silicide) process in which regions 40, 42, and 44 are formed of silicide. Sitaram teaches that silicide lowers the contact resistance (col. 5, ll. 30-35; col. 5, ll. 40-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to form a silicide region over the source/drain and gate in the process of Haken and Chu. A person of ordinary skill in the art would have been motivated to do this by the expectation that such a modification would lower the contact resistance of the device as suggested by Sitaram.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haken, Chu, and Sitaram as applied to claim 12 above, further in view of US 5,998,873 ("Blair").

Claim 13 requires forming a silicon dioxide layer over the silicide layer.

Blair teaches that interlevel dielectric layers are typically fabricated using silicide dioxide or silicon nitride (¶ bridging cols 3-4).

It would have been obvious to one of ordinary skill in the art to deposit a silicon dioxide layer over the silicide in the process of Haken, Chu, and Sitaram because silicon dioxide was a well known interlevel dielectric layer as taught by Blair.

Conclusion

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (571) 272-1848. The examiner can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (571) 272-1852.

The fax number for official correspondence is (703) 872-9306. Unofficial communications to the examiner may be faxed to (571) 273-1848. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

March 22, 2004
J. Vockrodt

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800